	DAY 1: December 3, 2024 (Tuesday)
08:00am - 08:55am	Registration
Venue	Grand Ballroom
09:00am - 09:15am	Opening Ceremony
09:15am - 10:00am	**Dr Vic Lin Jing-Cheng,** EVP, Samsung Electronics
	KEYNOTE: Unleashing AI Power: The Hybrid Copper Bonding Technology for 3D System Integration, HBM and CPO
10:00am - 10:45am	**Glenn G. Daves,** Senior VP, NXP Semiconductors
	KEYNOTE: Packaging at the Emerging Edge
10:45am - 11:00am	Coffee/Tea Break (Grand Ballroom Foyer)
11:00am - 12:30pm	Panel Session**: Asia's Role in the Global Semiconductor Industry** (Moderator: Keat Yap, Kearney)
	Panelist: Andrew Goh (Lam Research), Chan Pin Chong (Kulicke and Soffa)
12:30pm - 1:30pm	Lunch @ Grand Ballroom Foyer (Level 4)
Venue	Grand Ballroom
1:30pm - 2:15pm	**Dr Yu-Po Wang, VP,** Siliconware Precision Industries Co., Ltd.
	KEYNOTE: **Breaking Boundaries of IC Packaging through Innovative Integration Technology**
2:15pm - 3:00pm	**Tim Olson,** CEO, Deca Technologies
	KEYNOTE: Tectonic Forces Shaping the Future of the Semiconductor Industry
3:00pm - 3:45pm	**Dr Devan Iyer**, Chief Strategist (Advanced Packaging), IPC International
	KEYNOTE: Advanced Packaging-Customization Trends and Standardization Opportunities
3:45pm - 4:00pm	Tea Break & Exhibition (Grand Ballroom Foyer)
4:00pm - 5:30pm	Panel Session**: The Role of Co-Packaged Optics in Advancing AI Technologies** (Moderator: Matt Kelly/Dr Devan Iyer, IPC International Inc.)
	Panelist: Dr Masaki Kato (Marvell), Dr Torseten Wipiejewki (Huawei), Prof Subramanian S Iyer (UCLA), Dr Calvin Cheung (ASE) and PV Ramana (Lighspeed Photonics)
6:00pm - 8:00pm	**VIP Dinner (by invitation only)**

DAY 2: December 4, 2024 (Wednesday)						
Exhibition at Waterfromnt Foyer from 8:30am to 5:30pm (Level 2)						
Venue	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
09:00am - 10:45am	**PDC1: Chiplet, Heterogeneous Integration and Co-Packaged Optics**	**PDC2: Photonic Technologies for Communication, Sensing and Displays**	**PDC3: Wafer Bonding for Advanced Packaging Applications**	**PDC4: Current and Future Challenges and Solutions in AI & HPC**	**PDC5: Mechanics and Reliability of Lead-Free Solders Joints**	**PDC6: Failure Analysis of Advanced Packages: Fundamental, Skills, Philosophy & Case Studies**
	Dr John H. Lau Unimicron	Dr Torseten Wipiejewski Huawei	Dr Viorel Dragoi EV Group	Dr Refai-Ahmed Gamal AMD	Professor Jeff Suhling, Auburn Univeristy	Dr Yong-Fen Hsieh MA-Tek
10:45am - 11:00am	Coffee/Tea Break					
11:00am - 12:30pm	PDC1 (cont'd)	PDC2 (cont'd)	PDC3 (cont'd)	PDC4 (cont'd)	PDC5 (cont'd)	PDC6 (cont'd)
12:30pm - 2:00pm	EPS Luncheon @ Waterfront Ballroom (Level 2)					
2:00pm - 2:45pm	**Professor Subramanian S. Iyer**, Distinguished Professor, UCLA					
	KEYNOTE: **Strategic Directions for Electronics Packaging**					
2:45pm - 3:15pm	**Dr Victor Zhirnov**, Semiconductor Research Corporation (SRC)					
	TECHNOLOGY TALK: New Roadmap for Microelectronics: Charting the Semiconductor Industry's Path Over the Next 5, 10, and 20 Years					
3:15pm - 4:15pm	R10 Chaper Chairs' Meeting (Verando I)	Interactive Poster Presentation I / Exhibition / Coffee Break @ Waterfront foyer				
4:15pm - 6:00pm	Sponsors' Presentations & Lucky Draw @ Riverfront II and III					
6:00pm - 6:15pm	*Transport to EPTC Banquet Dinner*					
6:15pm - 9:00pm	**EPTC Banquet Dinner, RedDot BrewHouse @ Dempsey Hill**					

DAY 3: December 5, 2024 (Thursday AM)

Exhibition at Waterfront Foyer from 8:30am to 5:30pm (Level 2)

Venue	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
09:00am -09:30am	**Invited Talk 1: James Papanu, Tokyo Electron Limited** D2W Hybrid & Fusion Bonding to Enable Adv Packaging (P1313)	**Invited Talk 2: Tan Yik-Yee, Yole Group** Glass Core Substrate Market and Opportunity	**Invited Talk 3: Sidina Wane, eV-Technologies** Smart Integrated Electromagnetic Skins	**Invited Talk 4: Chan Pin Chong, Kulicke & Soffa** Fluxless TCB for Chiplet Integration	**Invited Talk 5: Chai Tai Chong, IME** RDL-First Interposer Technology for Next Generation Advanced Packaging	**Invited Talk 6: Hardik Kabaria, Vinci4D** Towards AI-Assisted Design of Thermal Management Strategies
09:30am -10:30am	**A1. Hybrid and Fusion Bonding 1**	**A2. Wafer Processing and Characterization**	**A3. Emerging Technologies I**	**A4. Advanced Packaging 1**	**A5. TSV and Wafer Level Packaging 1**	**A6. Thermal Management and Characterization 1**
09:30am - 09:50am	A1.1 (P1187) Improved Edge Detection Algorithm for Blurred Alignment Marks in Hybrid Bonding *Sugiura, Takamasa (1); Nagatomo, Daisuke (1); Kajinami, Masato (1);Ueyama, Shinji (1);Tokumiya, Takahiro (1);Oh, Seungyeol (2);Ahn, Sungmin (2);Choi, Euisun (2);Woo, Siwoong (2);Lee, Hyunjin (2);Lee, Byungjoon (2);Rhee, Minwoo Daniel (2)* Samsung Japan Corporation (1)	A2.1 (P1412) Comprehensive Die Strengths Comparisons for Glass using Different Singulation Methods *Wei, Frank* DISCO Corporation, USA	A3.1 (P1367) Trade-off between Chiplet Dimensions and Packaging Parameters for Optimal cost-performance for Chiplet Based Heterogenous Integration *Zhai, Max (1); Sahoo, Krutikesh (2); Iyer, Subramanian (2)* UCLA, USA (2)	A4.1 (P1262) Dual Damascene process for 500nm RDL using High Resolution Photosensitive Polymer *Gerets, Carine Helena; Pinho, Nelson; Tseng, Wen Hung; Paulus, Tinneke; Labyedh, Nouha; Beyer, Gerald; Miller, Andy; Beyne, Eric* IMEC, Belgium	A5.1 (P1344) Accelerating Overlay Error Optimization in Fine-Pitch Wafer-to-Wafer Hybrid Bonding through ML *James, Ashish (1); Venkataraman, Nandini (2); Miao, Ji Hong (2); Singh, Navab (2); Li, Xiaoli (1)* Institute for Infocomm Research, Singapore (1)	A6.1 (P1136) Thermal Design and Analysis of a Flip-Chip GaN-on-SiC HEMT *Feng, Huicheng; Zhou, Lin; Tang, Gongyue; Wai, Eva Leong Ching; Lim, Teck Guan* Institute of Microelectronics, Singapore
09:50am - 10:10am	A1.2 (P1195) Post-CMP Clean Optimization for SiCN Hybrid Bonding Applications *Ji, Hongmiao (1); LEE, Chaeeun (1);TEE, Soon Fong (1);TEO, Wei Jie (1);TAN, Gee Oon (1);Venkataraman, Nandini (1);Lianto, Prayudi (2);TAN, Avery (2);LIE, Joselyn (2);SUM, Darren (2);SEOW, Kevan (2);CHEOK, Kelvin (2);CHONG, Hoi Jin (2);TAMBOLI, Dnyanesh (3);TEO, Melvin (3)* Institute of Microelectronics, Singapore (1)	A2.2 (P1388) 200mm Reconstituted Wafer for Fan-out of Microfluidics and CMOS Electronics *Wei, Wei; Zhang, Lei; Tobback, Bert; Visker, Jakob; Stakenborg, Tim; Karve, Gauri; Tezcan, Deniz Sabuncuoglu* IMEC, Belgium	A3.2 (P1253) Feasibility and Performance of Fully Additive Manufactured Light Bulbs *Ankenbrand, Markus; Piechulek, Niklas; Franke, Jörg* Friedrich-Alexander Universität Erlangen Nürnberg, Germany	A4.2 (P1342) ECC-based Flux Cleaning Monitoring for Improved Reliability in Advanced Packaging Products *Wang, Yusheng; Huang, Baron; Lin, Wen-Yi; Zou, Zhihua; Kuo, Chien-Li* TSMC, Taiwan	A5.2 (P1373) Study of Direct Copper Electroplating on Ruthenium Seed Layer for TSV Processes at 300mm Wafer Level *Tran, Van Nhat Anh; Venkataraman, Nandini; Tseng, Ya-Ching; Chen, Zhixian* Institute of Microelectronics, Singapore	A6.2 (P1163) Silicon-Based Micro-Fluid Cooler Package Integration for High Performance Computing *Han, Yong; Tang, Gongyue; Lau, Boon Long* Institute of Microelectronics, Singapore
10:10am - 10:30am	A1.3 (P1369) Maximizing Productivity through Bonding Sequence Optimization in the Chip on Wafer Process *Kim, Junsang (1);Yun, Hyeonjun (1);Kang, Mingu (1);Cho, Kwanghyun (1);Cho, Hansung (1);Kim, Yunha (1);Moon, Bumki (1);Rhee, Minwoo (1);Jung, Youngseok (2);Lee, Byungjoon (1);Kwon, Ohwoon (2);Joung, Geewoong (2);Kim, Jisu (1);Lee, Jungchul (2)* Samsung Electronics, South Korea (1)	A2.3 (P1332) Diffraction Alignment Sensor and Mark Design Optimization to Enable Fine Overlay Accuracy for 50 um Thick Si Bonded to Glass *Tamaddon, Amir-Hossein (1); Jadli, Imene (1); Suhard, Samuel (1); Jourdain, Anne (1); Hsu, Alex (2); Schaap, Charles (2); De Poortere, Etienne (2); Miller, Andy (1); Kennes, Koen (1); Blanco, Victor (1)* IMEC, Belgium (1)	A3.3 (P1377) Innovations and Challenges in Laser Direct Structured Mechatronic Integrated Devices for Aviation *Piechulek, Niklas; Ankenbrand, Markus; Xu, Lei; Fröhlich, Jan; Nguyen, Huong Giang; Franke, Jörg* Lehrstuhl für Fertigungsautomatisierung und Produktionssystematik	A4.3 (P1256) Defluxing in Advanced Packaging: Critical Process Considerations and Solutions *Parthasarathy, Ravi* ZESTRON Americas	A5.3 (P1227) Utilizing Ensemble Learning on Small Database for Predicting the Reliability Life of Wafer-Level Packaging *Su, Qinghua (1); Yuan, Cadmus (2); Chiang, Kuo-Ning (1)* National Tsing Hua University, Taiwan (1)	A6.3 (P1103) Power Management IC device Efficiency & Thermal Study *Ge, Garry; Xu, L.Q.; Zhang, Bruce; Zeng, Dennis* NXP Semiconductor Company, China
10:30am - 10:45am	Tea Break & Exhibition (Waterfront Ballroom Foyer)					
Venue	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
10:45am -11:45am	**B1. Hybrid and Fusion Bonding 2**	**B2. Interconnection Technologies 1**	**B3. Thermal Interface Materials**	**B4. Advanced Packaging 2**	**B5. Assembly and Manufacturing Technology 1**	**B6. Thermal Management and Characterization 2**
10:45am - 11:05am	B1.1 (P1211) Next Generation of Thermo Compression Bonding Equipment *Abdilla, Jonathan* Besi, The Netherland	B.2.1 (P1221) Study of Solder Bump and Joint Standoff Height Profiles Using Empirical and Numerical Methods *Wang, Yifan; Yeo, Alfred; CHAN, Kai Chong* STATS ChipPac, Singapore	B3.1 (P1113) Evaluation of TIM Cross-Sectioning Methods on Lidded High-Performance Microprocessors *Neo, Shao Ming; Song, Mei Hui; Tan, Kevin Bo Lin; Lee, Xi Wen; Oh, Zi Ying; Foo, Fang Jie* AMD, Singapore	B4.1 (P1357) Investigation of UBM/RDL Contact Resistance Based on ICP Sputter Etch Conditions and Critical Design Dimensions *Carazzetti, Patrik (1); Drechsel, Carl (1); Haertl, Nico (1); Weichart, Jürgen (1); Viehweger, Kay (2); Strolz, Ewald (1)* Evatec AG, Switzerland (1)	B5.1 (P1230) Investigation Of Multi Beam Laser Grooving Process And Die Strength for 55nm Code Low-k Wafer *Xia, Mingyue; Wang, Jianhong; Xu, Sean; Li, guangming; Liu, haiyan; Zhu, lingyan* NXP, China	B6.1 (P1274) Real-time Evaluation of Effective Thermal Conductivity Profile for the Redistribution Layer (RDL) *Liu, Jun; Li, Yangfan; Cao, Shuai; Sridhar, N.* IHPC, A*STAR, Singapore
11:05am - 11:25am	B1.2 (P1316) Parylene as an adhesive for wafer and chip bonding as well as for applications in wafer level packaging *Selbmann, Franz (1,2); Kühn, Martin (1,2); Roscher, Frank (1); Wiemer, Maik (1); Kuhn, Harald (1,3); Joseph, Yvonne (2)* Fraunhofer Institute for Electronic Nano Systems, Germany (1)	B2.2 (P1134) Solder Ball Alloy Effect on Board Level Reliability Thermal Cycling and Vibration Test Enhancement *Chen, Fa-Chuan (1); Yu, Kevin (1); Lin, Shih-Chin (1); Chu, Che-Kuan (2); Lin, Tai-Yin (2); Lin, Chien-Min (2)* Mediatek, Taiwan	B3.2 (P1125) Analysis of Indium-Silver Alloy Thermal Interface Material Reliability and Coverage Degradation Mechanisms *Park, Donghyeon* Amkor, Korea	B4.2 (P1389) Precise Wavelength Control in Fabry-Perot Filters using Thin Etch Stop Layers *Babu Shylaja, Tina; Tack, Klaas; Sabuncuoglu Tezcan, Deniz* IMEC, Belgium	B5.2 (P1215) An Optimization Study with Batch Microwave Plasma On Extra *LOO, Shei Meng; LEONE, Federico; CAICEDO, Nohora* STMicroelectronics, France	B6.2 (P1282) POD-ANN Thermal Modelling Framework for Rapid Thermal Analysis of 2.5D Chiplet Designs *Li, Yangfan; Liu, Jun; Cao, Shuai; Sridhar, Narayanaswamy* IHPC, A*STAR, Singapore
11:25am - 11:45am	B1.3 (P1368) Process Development of Chip to Wafer Hybrid Bonding with Polymer Passivation *Xie, Ling* Institute of Microelectronics, Singapore	B2.3 (P1185) Navigating the Optimal Material Selection for RF Transmission Lines in Cryogenic Systems *Lau, Daniel (1); Bhaskar, Vignesh Shanmugam (1); Ng, Yong Chyn (1); Zhang, Yiyu (2); Goh, Kuan Eng Johnson (2); Li, Hongyu (1)* Institute of Microelectronics, Singapore	B3.3 (P1225) Selection of Non-clean Flux for Metal TIM *Li, Dai-Fei; Teng, Wen-Yu; Hung, Liang-Yih; Kang, Andrew; Wang, Yu-Po* Siliconware Precision Industries Co., Ltd., Taiwan	B4.3 (P1348) Packaging technology for Sub-terahertz antenna in module *Murayama, Kei (1); Taneda, Hiroshi (1); Tsukahara, Makoto (1); Hasaba, Ryosuke (2); Morishita, Yohei (2); Nakabayashi, Yoko (1)* Shinko Electric Industries Co.,Ltd, Japan (1)	B5.3 (P1255) In-situ Characterization of Plasma Species for Process Optimization and Improvement *Chou, Djamila; Capellaro, Laurence; Caicedo, Nohora* STMicroelectronics, France	B6.3 (P1171) Effect of Contact Characteristics on Thermal Contact Resistance of Grease-less Uniform Contact Surfaces *Aoki, Hirotoshi (1); Fushinobu, Kazuyoshi (2); Tomimura, Toshio (3)* KOA Corporation, Japan (1)
11:45am -1:00pm	**EPTC Luncheon @ WaferFront Ballroom (Level 2)**					

DAY 3: December 5, 2024 (Thursday PM)

Exhibition at Waterfront Foyer from 8:30am to 5:30pm (Level 2)

Venue	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
1:00pm - 2:00pm	**C1. Electrical Simulations & Characterization 1**	**C2. Wireless and Antenna Package Designs**	**C3. Materials and Processing 1**	**C4. Mechanical Simulation & Characterization 1**	**C5. TSV and Wafer Level Packaging 2**	**C6. Thermal Management and Characterization 3**
1:00pn - 1:20pm	C1.1 (P1108) Signal integrity analysis of dense wire channels on 2.5D substrate technologies for UCIe and BOW applications *Rotaru, Mihai Dragos* Institute of Microelectronics, Singapore	C2.1 (P1397) A Compact 1x4 Antenna Array with Steerable Beam for 5G millimeter-Wave Smartphone Applications *Hsieh, Sheng-Chi* ASE Group, Taiwan	C3.1 (P1159) Photosensitive aqueous alkaline developable magnetic material for inductor and balun transformers in 3D WLP *Masuda, Seiya; Idei, Hiroaki; Miyata, Tetsushi; Oi, Shota; Suzuki, Hiroyuki* FUJIFILM Corporation, Japan	C4.1 (P1324) Copper balance and wafer level warpage control and effect of package stress and board-level TC solder joint reliability *Mandal, Rathin* Institute of Microelectronics, Singapore	C5.1 (P1396) Advantages of Digital Lithography in Patterning of UHD FoWLP Utilizing Novel PI Dielectrics *Varga, Ksenija* EV Group, Austria	C6.1 (P1354) Efficient Thermal-Aware Floor-planning with Bayesian Optimization: A Simulation-Efficient Approach *Hegedüs, János; Takács, Dalma; Hantos, Gusztáv; Poppe, András* Institute for Infocomm Research, Singapore
1:20pm - 1:40pm	C1.2 (P1161) Design of Underground Structure Cover with Self-Complementary Slits for Wireless Telecommunication Application *Rong, Zihao (1); Yi, Yuantong (1); Tateishi, Eiichi (2); Kumagae, Takaya (2); Kai, Nobuhiro (2); Yamaguchi, Tatsuya (3); Kanaya, Haruichi (1)* Kyusu University, Japan (1)	C2.2 (P1139) Development of 2.4GHz band L-shaped Circular Polarized slot antenna *Suehiro, Kazuki; Nakashima, Kenta; Kanaya, Haruichi* Kyushu University, Japan	C3.2 (P1118) New DA Adhesive Meets Challenging Performance, Reliability and Cost Objectives of Automotive MCU Packaging *Kang, Jaeik; Hong, Xuan; Zhuo, Qizhuo; Yun, Howard; Shim, Kail; Rathnayake, Lahiru; Surendran, Rejoy; Trichur, Ram* Henkel, USA	C4.2 (P1340) Material sensitivity of a fan-out package warpage – simulations and experimental validation *Tippabhotla, Sasi Kumar; Soon Wee, David Ho* Institute of Microelectronics, Singapore	C5.2 (P1193) Chip to Wafer and Wafer to Wafer Density estimation and Design rules physical verification. *Mani, Raju; Dutta, Rahul; Cheemalamarri, Hemanth Kumar; Vasarla Nagendra, Sekhar* Institute of Microelectronics, Singapore	C6.2 (P1343) Optimizing Chiplet Placement in Thermally Aware Heterogeneous 2.5D Systems Using Reinforcement Learning *Kundu, Partha Pratim (1); Furen, Zhuang (1); Sezin, Ata Kircali (1); Yubo, Hou (1); Dutta, Rahul (2); James, Ashish (1)* Institute for Infocomm Research, Singapore (1)
1:40pm - 2:00pm	C1.3 (P1167) Equivalent Electromagnetic Radiation Model of Chip Based on Near-Field Scanning for EMI Analysis in Ceramic SiP *Liang, Yaya; Du, Pingan* UESTC, China	C2.3 (P1203) Development of Long-Range Wireless Energy Harvesting Circuit by Multistage Cockcroft-Walton Circuit *Tagawa, Nobuya; Hosaka, Ryoma; Tanaka, Hayato; fGoodwill, Kumar; Kanaya, Haruichi* Kyushu University, Japan	C3.3 (P1246) Doped SAC Solder Ball Alloys Comparison for High Performance Automotive BGA Packages *Grolier-lee, Stelliane (1); Capellaro, Laurence (1); Mon, Aye aye (2); Wong, Kim-Sing (2); Loh, Hung-Meng (2); Caicedo, Nohora (1)* STMicroelectronics, France (1)	C4.3 (P1147) Advanced Prediction Model for SACQ Solder Reliability Assessment for Automotive Memory Applications *Pan, Ling (1); Che, Faxing (1); Ong, Yeow Chon (1); Yu, Wei (1); Ng, Hong wan (1); Kumar, Gokul (2); Fan, Richard (3); Hsu, Pony (3)* Micron Semiconductor Asia Operations, Singapore (1)	C5.3 (P1374) Panel Level Fine Patterning RDL Interposer Package *Park, Jieun; Kim, Dahee; Choi, Jaeyoung; Park, Wooseok; Choi, Younchan; Lee, Jeongho; Choi, Wonkyoung* Samsung Electronics, South Korea	C6.3 (P1259) From Package Thermal Measurements to Material Characterization: A Remote Phosphor Aging Test *Zhuang, Furen (1); Pratim Kundu, Partha (1); Kircali Sezin, Ata (1); Hou, Yubo (1); Dutta, Rahul (2); James, Ashish (1)* Budapest University of Technology and Economics (1)
2:00pm - 3:00pm	Interactive Poster Presentation II / Exhibition / Coffee Break @ Waterfront foyer				Heteregeous Integration Roadmaps (HIR) Workshop (3:15pm to 5:20pm)	
3:00pm - 4:20pm	**D1. Electrical Simulations & Characterization 2**	**D2. Interconnection Technologies 2**	**D3. Materials and Processing 2**	**D4. Mechanical Simulation & Characterization 2**		
3:00pm - 3:20pm	D1.1 (P1272) Crosstalk Analysis for Symmetric and Asymmetric High-Speed Signal Lines of GDDR6 Package *Jaiswal, Anushruti (1); Krishna, Vamsi (1); Dhanekula, Mahesh Babu (1); Desmond Dsilva, Hansel (2)* Ansys, India (1)	D2.1 (P1146) Assembly of Multi-Device Power Package with Clips as Interconnects *Wai, Leong Ching; Yeo, Yi Xuan; Soh, Jacob Jordan; Tang, Gongyue* Institute of Microelectronics, Singapore	D3.1 (P1137) Novel Residue free High Lead Solder Paste for Power discrete *Bai, Jinjin; Li, Yanfang; Liu, Xinfang; Chen, Fen; Liu, Yan* Indium, China	D4.1 (P1205) Impact of Structural Parameters on the Warpage of fcBGA Packages with Indium Thermal Interface Material *Liu, Zhen (1); Dai, Qiaobo (1); Nie, Linjie (1); Xu, Lanying (1); Teng, Xiaodong (1); Zheng, Boyu (1,2)* Changsha AnMuQuan Intelligent Technology, China (1)		
3:20pm - 3:40pm	D1.2 (P1355) Signal Integrity Simulation and Analysis for 2.5D Advanced Package Interconnect Based on UCIe *Fan, Yuxuan (1,2); Gan, Hanchen (1,2); Zhou, Yunyan (1); Lei, Bo (1); Song, Gang (1); Wang, Qidong (1)* IMECAS, China (1)	D2.2 (P1129) Characterization of Recycleed Gold Bonding Wire on Memory Package *Chen, Yi-jing; Zou, Yung-Sheng; Chung, Min-Hua; Gan, Chong-Leong* Micron, Taiwan	D3.2 (P1220) Low Flux Residue No-Clean Solder Paste for System-in-Package (SiP) Application *Liu, Xinfang; Bai, Jinjin; Chen, Fen; Liu, Yan* Indium, China	D4.2 (P1141) Impact of Package Warpage on Package Strength Assessment under Three-Point Bending Test Condition *Che, Fa Xing (1); Ong, Yeow Chon (1); Yu, Wei (1); Pan, Ling (1); Ng, Hong Wan (1); Kumar, Gokul (2); Takiar, Hem (2)* Micron Semiconductor Asia Operations, Sinagpore (1)		
3:40pm - 4:00pm	D1.3 (P1223) Effect of Mesh Ground Plane on Impedance Control and Crosstalk of Organic Interposers Targeted for Chiplet Applications *Lim, Ying Ying (1); Nemoto, Shunsuke (2)* National Institute of Advanced Industrial Science and Technology, Japan (1)	D2.3 (P1126) Investigation of the Electromigration Behaviour of Solder Bump under Different Conditions *Law, Yi Kei Owen (1); Fan, Haibo (1); Zhong, Chenchao Nick (1); Shi, Yuning (2)* Nexperia, Hong Kong	D3.3 (P1176) Analysis of Basic Properties and Bonding Properties of Various Melting Temperature Solders *Kim, Hui Joong; Lee, Jace; Lee, Seul Gi; Son, Jae Yeol; Won, Jong Min; Park, Ji Won; Kim, Byung Woo; Shin, Jong Jin; Lee, Tae Kyu* MKE, South Korea	D4.3 (P1181) Evaluation of Thermo-mechanical Fatigue life of Microvias under PCB Substrate's influence during Reflow Process *Syed, Mujahid Abbas; Yu, Qiang* Yokohama National University, Japan		
4:00pm - 4:20pm	D1.4 (P1241) Development of Compact Wideband Balun using Multilayer Substrate-integrated Coaxial line *Sato, Takumi (1); Kanaya, Haruichi (1); Ichirizuka, Takashi (2); Yamada, Shusaku (2)* Kyushu University, Japan (1)	D2.4 (P1168) Investigation of NiSn4 formation in the Relation between SnBi Solder and ENEPIG Substrate *Wang, Yi-Wun; Tsai, Cheng-Ting; Lin, Tzu-Yi* Tamkang University, Taiwan	D3.4 (P1124) A Novel Method for PBO Adhesion Characterization in WLCSP Package *CHEN, Yong; CHANG, Jason; GANI, David; LUAN, Jing-en; CATTARINUZZI, Emanuele* STMicroelectronics, Singapore	D4.4 (P1160) Improved Thermal performance of 3D Opto-Electronic IC assembled on multiple Interposers through design optimization *Rekapalli, Vamsi (2); Mohammed, Ubed (2); V Ramana, Pamidighantam (1); Yeluripati, Rohin Kumar (1); Bhandari, Jugal Kishore (2); Dharavath, Sandhya (2)* Lightspeed Photonics, Singapore		
4:20pm - 5:20pm	**Exhibitors' Presentations & Luckly Draw @ Riverfront II and III**					
5:30pm - 7:00pm	**Sponsor & Exhibitors Appreciation / Networking Session (by invitation only)**					

DAY 4: December 6, 2024 (Friday AM)

Exhibition at Waterfront Foyer from 8:30am to 4:30pm (Level 2)

Venue	Waterfront I	Waterfront II	Waterfront III	Riverfront I	Riverfront II	Riverfront III
09:00am -10:20am	**E1. Assembly and Manufacturing Technology 2**	**E2. Emerging Technologies 2**	**E3. Materials and Processing 3**	**E4. Mechanical Simulation & Characterization 3**	**E5. Quality, Reliability & Failure Analysis 1**	**E6. Silicon Interposer and Processing**
09:00am - -9:20am	E1.1 (P1175) Investigation on Molding Void Issue in System-in-Package Module *Yang, Chaoran; Tang, Oscar; Song, Fubin* Amazon, China	E2.1 (P13520) CMOS compatible 2D material integration for Sensor Applications on 200mm wafers *Yoo, Tae Jin; Tezcan, Deniz Sabuncuoglu* IMEC, Belgium	E3.1 (P1247) Study on Microstructure and Mechanical Properties of Silver and Silver-Indium Solid Solution Films Using Magnetron Sputtering *Zhao, Shuang (1); Lin, Pengrong (2,3); Zhang, Donglin (1); Wang, Taiyu (1);* *Liu, Sichen (1); Xie, Xiaochen (2); Xu, Shimeng (2); Qu, Zhibo (2); Wang, Yong (2); Zhao, Xiuchen (1); Huo, Yongjun (1,4)* Beijing Institute of Technology, China (1)	E4.1 (P1121) Analytical K-factor Model for Monotonic Four-point Bend Test Design *Kelly, Brian (1); Tarnovetchi, Marius (2); Newman, Keith (1)* AMD, USA (1)	E5.1 (P1164) Non-Destructive Analysis of Voiding in TIM of High-Performance Computing Devices using B-mode Scanning *Song, Mei Hui; Tang, Wai Kit; Tan, Li Yi* AMD, Singapore	E6.1 (P1207) Adaptive Pad Stacks Deliver Order of Magnitude Increase in Bridge Die Position Tolerance in Embedded Fan-out Interposers *Sandstrom, Clifford Paul (1); Talain, John Erickson Apelado (1); San Jose, Benedict Arcena (1); Fang, Jen-Kuang (2); Yang, Ping-Feng (2); Huang, Sheng-Feng (2); Shen, Ping-Ching (2)* Deca Technologies, USA (1)
9:20am - 9:40am	E1.2 (P1172) Enhancing DI Water Cleanability of Tacky Flux on Cu OSP Surface Using FC Copper Pillar High-Density Interconnection *Lip Huei, Yam; Risson Olakkankal, Edrina; Balasubramanian, Senthil KUmar* Heraeus Materials Singapore	E2.2 (P1384) Hyperspectral Component Fabrication on 200mm CMOS Image Sensor Wafer *Babu Shylaja, Tina; Yoo, Tae Jin; Geelen, Bert; Tack, Klaas; Sabuncuoglu Tezcan, Deniz* IMEC, Belgium	E3.2 (P1206) Versatile Photosensitive Polymer Applied in Low-Temperature Hybrid Bonding with Nanocrystalline Cu *Tan, Chung-An (1); Lee, Chia-Hsin (1); Lee, Ou-Hsiang (2); Chiu, Wei-Lan (2);* *Chang, Hsiang-Hung (2); Yu, Shih-cheng (2)* Brewer Science, Taiwan	E4.2 (P1135) Enhancing Mechanical Robustness and Integrity of a Large Advanced Package with Embedded FP Interconnect Chips *Ji, Lin; Chai, Tai Chong* STMicroelectronics, Singapore	E5.2 (P1361) A Method for Die-level Fracture Toughness Evaluation by Nano-Indentation on Ring *Zhu, Xintong; Rajoo, Ranjan; Nistala, Ramesh Rao; Mo, Zhi Qiang* Globalfoundries, Singapore	E6.2 (P1119) Silicon Interposer Heterogenous Integration Platform for Millimeter Wave Ka and V band Satellite Applications *Sun, Mei; Ong, Javier Jun Wei; Wu, Jia Qi; Lim, Sharon Pei Siang; Ye, Yong Liang; Umralkar, Ratan Bhimrao; Lau, Boon Long; Lim, Teck Guan; Chai, Kevin Tshun Chuan* Institute of Microelectronics, Singapore
9:40am - 10:00am	E1.3 (P1326) Film Assisted Molding Performance Improvement with Component Design *Law, Hong Cheng; Lim, Fui Yee; Low, Boon Yew; Pang, Zi Jian; Bharatham, Logendran; Yusof, Azaharudin; Ismail, Rima Syafida; Lim, Denyse Shyn Yee; Lim, Shea Hui* NXP, Malaysia	E2.3 (P1390) Characterization of Carbon Contained Films at Bonding Interface for the Application of Backside Power Delivery Networks *Kitagawa, Hayato; Sato, Ryosuke; Fuse, Junya; Yoshihara, Yuki; Inoue, Fumihiro* Yokohama National University, Japan	E3.3 (P1286) Low temperature Ag sintering and driving force on Au finished Cu substrates at 145°C and 175°C using Ag nano-porous sheets without organic solvents *Kim, YehRi (1,2); Yu, Hayoung (1); Noh, Seungjun (3); Kim, Dongjin (1)* Korea Institute of Industrial Technology (1)	E4.3 (P1116) Study on Substrate Copper Pad Crack Through Experiment and Simulation *Yu, Wei; Che, Fa Xing; Ong, Yeow Chon; Pan, Ling; Cheong, Wee Gee* Micron Semiconductor Asia Operations, Singapore	E5.3 (P1140) Electrostatically induced voltage generated in different type boxes of electronic equipment by moving charged object *Ichikawa, Norimitsu* Kogakuin University, Japan	E6.3 (P1138) Development of Large RDL Interposer Package: RDL-first FOWLP and 2.5D FO-Interposer *Ho, Soon Wee David; Soh, Siew Boon; Lau, Boon Long; Hsiao, Hsiang-Yao;* *Lim, Pei Siang; Rao, Vempati Srinivasa* Institute of Microelectronics, Singapore
10:00am - 10:20am	E1.4 (P1224) An Investigation of Different Leadframe Materials with Plasma Cleaning on Extra-Large Leadframe to Study the Effects of Oxidation vs Delamination *CHUA, Yeechong; CHUA, Boowei; LEONE, Federico; LOO, Shei Meng* STMicroelectronics, Singapore	E2.4 (P1376) Screen Printed Temperature Sensor using Novel Kish Graphite/reduced Graphene Oxide Conductive Ink for Wearable Applications. *Rao, Ankitha (1); Bhat, Somashekara (1); De, Shounak (1); Shetty K, Nakul (1); Nayak, Ramakrishna (2)* Manipal Institure of Technology, India (1)		E4.4 (P1130) Predictive Numerical Modeling of Stealth Dicing Process for Different Wafer Pre-Thin Thicknesses *Lim, Dao Kun (1,2); Vempaty, Venkata Rama Satya Pradeep (2); Shah, Ankur Harish (2); Sim, Wen How (2); Singh, Harjashan Veer (2); Lim, Yeow Kheng (1)* Micron Technology, Singapore (1)	E5.4 (P1350) High spatial resolution imaging of dopants and impurities for semiconductor device using NanoSIMS *Sameshima, Junichiro; Nakata, Yoshihiko; Akahori, Seishi; Hashimoto, Hideki; Yoshikawa, Masanobu* Toray Research Center, Inc, Japan	E6.4 (P1209) Modeling and Fabrication of Silicon Integrated Multi-terminal Deep Trench Capacitor Technology *Lin, Weida (1); Song, Changming (2); Shao, Ziyuan (3); Ma, Haiyan (2); Cai, Jian (2,4); Gao, Yuan (1); Wang, Qian (2,4)* Tsinghua University, China (1)
10:20am - 10:35am	Tea Break & Exhibition (Waterfront BallRoom Foyer)					
10:35am -11:55am	**F1. Automotive and Power Device Packages**	**F2. Quality, Reliability & Failure Analysis 2**	**F3. Materials and Processing 4**	**F4. Advacned Optoelectronics**	**F5. Electrical Simulations & Characterization 3**	**F6. Thermal Management and Characterization 4**
10:35am -10:55am	F1.1 (P1234) A Highly Integrated AiP Design for 6G Application *WU, PO-I; Kuo, Hung-Chun; Jhong, Ming-Fong; Wang, Chen-Chao* ASE Group, Taiwan	F2.1 (P1184) Optimization of Aluminium Wirebonding on Niobium for Cryogenic Packaging *Norhanani Jaafar* Institute of Microelectronics, Singapore	F3.1 (P1254) Study of Interactions between RDL Polyimides and Underfills on Reliability of Flip-Chip Interconnects in Thermal Cycling *Chang, Hongda (1); Soriano, Catherine (1); Chen, WenHsuan (1); Yang, HungChun (2); Lai, WeiHong (2); Chaware, Raghunandan (1)* Lattice Semiconductor Corp, Taiwan	F4.1 (P1252) Aerosol Jet Printed Encapsulation for Optoelectronics: A Study of Line Morphology *Siah, Kok Siong (1); Basu, Robin (2); Distler, Andreas (2); Häußler, Felix (1);* *Franke, Jörg (1); Brabec, Christoph J. (2,3,4); Egelhaaf, Hans-Joachim (2,3,4)* Friedrich-Alexander Universität Erlangen Nürnberg, Germany (1)	F5.1 (P1201) Effect of Decoupling Capacitor Location on PDN Impedance in fcBGA Packages *Song, Xiaoyuan (1); Zheng, Boyu (1,2); Luo, Jiahu (1); Wei, Ping (1); Liu, Lei (1)* Changsha Anmuquan, China (1)	F6.1 (P1258) Thermal Characterization of LED Packages Covered with Wavelength Converting Phosphor Over a Large Area *Hantos, Gusztáv; Hegedüs, János; Lipák, Gyula; Németh, Márton;Poppe, András* Budapest University of Technology and Economics
10:55am - 11:15am	F1.2 (P1298) Packaging-Codesign for the development of a high-resolution MIMO-Radar-Module for Automated guided vehicles *Tschoban, Christian; Pötter, Harald* Fraunhofer IZM, Germany	F2.2 (P1182) In-Situ Microcrack Localization and Imaging in Laminated Die-Attachment Based on the Static Component of Ultrasonic Lamb Waves *Long, Xu (1); Li, Yaxi (2); Wang, Jishuo (3); Zhao, Liang (3); Yuan, Weifeng (3)* Northwestern Polytechnical University, China	F3.1 (P1179)An Innovative Flux-Less Solder Ball Attachment Technology (FLAT) for Advanced BGA Assembly *Kim, Dongjin (1); Han, Seonghui (1,3); Han, Sang Eun (1,4); Choi, Dong-Gyu (1,5); Chung, Kwansik (2); Kim, Eunchae (2); Yoo, Sehoon (1)* Korea Institute of Industrial Technology (1)	F4.2 (P1341) Quantum Cascade Laser Integration with Mid-Infrared Photonic Integrated Circuits for Diverse Sensing Applications *Kannojia, Harindra Kumar (1); Zhai, Tingting (1); Maulini, Richard (2); Gachet, David (2); Kuyken, Bart (1); Van Steenberge, Geert (1)* IMEC, Belgium (1)	F5.4 (P1200) A Novel Approach to Reduce Impedance Discontinuities for High-speed Channel in IC Packages Luo, Jiahu (1); zheng, Boyu (1,2); Song, Xiaoyuan (1); Jiang, Bo (1); Lee, SooLim (1) Changsha Anmuquan, China	F6.2 (P1289) Numerical Optimization of PCM-Based Heat Sink for Thermal Management of High-power-density Electronics *HU, RAN (1,2); Du, Jianyu (2); Shi, Shangyang (1,2); Lv, Peijue (1,2); Cao, Huiquan (2); Jin, Yufeng (1,2); Zhang, Chi (2,3,4); Wang, Wei (2,3,4)* Peking University, China
11:15am - 11:35am	F1.3 (P13060) Robustness Methodology for Next Generation Automotive Microcontroller Flip Chip Copper Pillar Technologies *Tan, Aik Chong; Bauer, Robert; Rau, Ingolf; Doering, Inga* Infineon Technologies, Singapore	F2.3 (P1122) BLR Drop Test Study for FCCSP Package with OSP/Cu Solder Pad finish *Liu, Jinmei* NXP Semiconductor Company, China	F3.3 (P1281) Elimination of Parametric Shifts in Trench MOSFETs Using Low Alpha-Particle Solder *Gajda, Mark A. (1); de Leon, Charles Daniel T. (2);* *A/P Ramalingam, Vegneswary (3); Santican, Haima (3)* Nexperia, United Kingdom	F4.3 (P1328) III-V Laser Diode Flip Chip Bonding on Photonics Integrated Circuit with SnAg Solder *Chi, Ting Ta (1); Ser Choong, Chong (1); Lee, Wen (1); Yuan, Xiaojun (2)* Institute of Microelectronics, Singapore (1)	F5.3 (P1304) Full-Wave Electromagnetic Simulation Approach for Integrated 3D-IC Design *Jaiswal, Anushruti; Patil, Tejkiran; Dhanekula, Mahesh Babu* Ansys, India	F6.3 (P1269) Heat-Resistant Reliability of Large Area Silver Microporous Connections for Direct Cooling in Power Inverter Applications *Yu, HaYoung; Kim, Seoah; Kim, Dongjin* Korea Institute of Industrial Technology
11:35am - 11:55pm	F1.4 (P1387) Bond Strength Comparison of Commercial and Custom Copper Sinter Pastes under Sinter Process Modifications *Meyer, Meyer; Gierth, Karl Felix Wendelin;Meier, Karsten; Bock, Karlheinz* Technische Universität Dresden, Germany	F2.4 (P1236) Influence of Material Composition on Copper-aluminum Wire Bonding Reliability *Carluccio, Roberta (1); Caglio, Carolina (1); Alesi, Mirko (1); Mancaleoni, Alberto (1); Villa, Riccardo (1); Serafini, Andrea (1); Dellasega, David (2)* STMicroelectronics, Italy (1)	F3.4 (P1218) Effects of Bi contents in Sn–5Ag lead-free solders on mechanical properties and morphology of IMC *Liu, Kuan Cheng; Li, Chuan Shun; Teng, Wen Yu; Hung, Liang Yih; Wang, Yu Po* Siliconware Precision Industries Co., Ltd., Taiwan	F4.4 (P1128) Generation of Beam Profiles from Chip-to-Free-Space Coupling using Deep Neural Network *Lim, Yu Dian (1); Tan, Chuan Seng (1,2)* Nanyang Technological Univeristy, Singapore (1)	F5.2 (P1162) Discussion on the Electrical Characteristics of Tera-Hz in Organic Substrate *Lin, Ho-Chuan; Lai, Chia-Chu; Shih, Teny; Kang, Andrew; Wang, Yu-Po* Siliconware Precision Industries Co., Ltd., Taiwan	F6.4 (P1199) A Study on Thermal Performance Enhancement for Multi-chip Power µModules *Dai, Qiaobo (1); Liu, Zhen (1); Liao, Linjie (2); Zheng, Boyu (1,3); Liu, Zheng (1); Yuan, Sheng (1)* Changsha Anmuquan, China (1)
11:55am - 12:55pm	Young Professionals' Event	**Event Lunch @ WaferFront Foyer (Level 2)**				

DAY 4: December 6, 2024 (Friday PM)

Exhibition at Waterfront Foyer from 8:30am to 4:30pm (Level 2)

Venue	Waterfront I	Waterfront II	Waterfront III	Riverfront I	Riverfront II	Riverfront III
12:55pm - 2:15pm	**G1. Bonding & Debonding Processes**	**G2. Wafer Processing and Characterization 2**	**G3. Materials and Processing 5**	**G4. Smart Manufacturing, Equipment & Tooling Co-Design**	**G5. TSV and Wafer Level Packaging 3**	**G6. Embedded and Fan-Out Packaging**
12:55pm - 01:15pm	G1.1 (P1380) High-temp-stable temporary bond adhesive for IR laser debonding enables new process integration for thin wafers *Koch, Matthew (1); kumar, Amit (1); Brandl, Elisabeth (2); Bravin, Julian (2); Urban, Peter (2); Geier, Roman (3); Siegert, Joerg (3)* Brewer Science, United Kingdom (1)	G2.1 (P1411) Patterning of 1µm Critical Dimension Through Silicon Via using Positive Tone Resist Mask by a Photolithography Stepper *Sundaram, Arvind (1); Kang, Riley (2); Bhesetti, Chandra Rao (1)* Institute of Microelectronics, Singapore (1)	G3.1 (P1198) Influence of Flow Rate and Current Density on Copper Deposition in Through Hole *Zeng, Barry; Ye, Rick; Pai, Yu-Cheng; Wang, Yu-Po* Siliconware Precision Industries Co., Ltd., Taiwan	G4.1 (P1309) Exploring Diffusion Model for Semiconductor Defect Detection *Lu, Kangkang; Cai, Lile; XU, Xun; Pahwa, Ramanpreet; Wang, Jie; Chang, Richard; Foo, Chuan-Sheng* Institute for Infocomm Research, Singapore	G5.1 (P1180) Optimization of High Aspect Ratio Copper Pillar Fabrication for Through Mold Interposer (TMI) Processing *Peh, Cun Jue; Lau, Boon Long; Chia, Lai Yee; Ho, Soon Wee.* Institute of Microelectronics, Singapore	G6.1 (P1202) Integration Module of Dual MOSFET Switching Circuit Using Embedded Silicon Fan-Out (eSiFO®) Technology *Qiang, Wenbin; Zhang, Xiangou; Sun, Xiangyu; Deng, Shuairong; Yang, Zhenzhong* Microsystem and Terahertz Research Center, China
01:15pm - 01:35pm	G1.2 (P1250) Delamination of Temporary Bonded Wafers: A Comprehensive Study *Jedidi, Nader* IMEC, Belgium	G2.2 (P1410) Niobium- last Process for Multi-foundry-compatible Wafer Level Processing of Superconducting Interposers *Goh, Simon Chun Kiat; Ng, Yong Chyn; Ong, Javier Jun Wei; Lau, Daniel; Tseng, Ya-Ching; Jaafar, Norhanani; Yoo, Jae Ok; Liu, Liyuan; Teo, Everline Shu Yun; Chua, Nicholas Boon Leong; Li, Hongyu* Institute of Microelectronics, Singapore	G3.2 (P1156) Routable Wettable Flanks for MEMS devices *Shaw, Mark; Gritti, Alex; Ratti, Andrea; Wong, Kim-Sing; Loh, Hung-meng; Casati, Alessandra; Antilano Jr, Ernesto; Soreda, Alvin* STMicroelectronics, Italy	G4.2 (P1287) End-to-end Fast Segmentation Framework for 3D Visual Inspection of HBMs *Wang, Jie (1); Chang, Richard (1); Lim, Meng Keong (2); Chong, Ser Choong (2); Yang, Xulei (1); Pahwa, Ramanpreet Singh (1)* Institute for Infocomm Research, Singapore (1)	G5.2 (P1405) Splitting Process Integration for 2.5D/3D Packaging *Li, Hongyu (1); Vasarla Nagendra, Sekhar (1); Schwarzenbach, Walter (2); Besnard, Guillaume (2); Lim, Sharon (1); BEN MOHAMED, Nadia (2); Nguyen, Bich-Yen (2)* Institute of Microelectronics, Singapore	G6.2 (P1268) Corrosion behavior of aluminium pads in Fan-Out Panel Level Packaging (FOPLP) *Yu, Yeonseop (1); Park, Seyoon (2); Kim, Miyang (2); Moon, Taeho (1)* Samsung Electronics, South Korea (1)
01:35pm - 01:55pm	G1.3 (P1192) Surface Quality Challenges Associated with Temp Bonding and Debonding for Chip Stacking Applications *Chaki Roy, Sangita; Vasarla, Nagendra Sekhar; Venkataraman, Nandini* Institute of Microelectronics, Singapore	G2.3 (P1331) A New D2W Bonding Alignment Scheme using Magnetic and Capillary assisted Self-alignment *Choi, Daesan (1); Kim, Sumin (2); Hahn, Seung Ho (1); Moon, Bumki (1); Rhee, Daniel Minwoo (1)* Samsung Electronics, South Korea	G3.3 (P1183) Understanding and Improving Rc Management for Wafer Level Packaging through Novel PVD Processing *Barker, Anthony James; Haymore, Scott; Wilby, Tony; Rastogi, Amit; Moncrieff, Ian; Jones, Steve; Joanne Chuan Sun* KLA-Tencor, United Kindom	G4.3 (P1375) Ultra-thin ta-C Hermetic Seals for Electronics Packaging *Phua, Eric Jian Rong; Lim, Song Kiat Jacob; Tan, Yik Kai; Shi, Xu* Nanofilm Technologies, Singapore	G5.3 (P1285) Fabrication of Through Alumina Vias: A Cost-effective Alternative Approach Using Ultrasonic Machining and Electroless Deposition *Pawar, Karan; Pandey, Harsh; Dixit, Pradeep* Indian Institute of Technology Bombay	G6.3 (P1123) Comparison of Electrical, Thermal, and Mechanical Performances of a fcBGA with that of a Fan-Out SiPlet Package *Ouyang, Eric; Ahn, Billy; Han, BJ; Han, Michael; Kang, Chen; Oh, Michael* Silicon Box
01:55pm - 02:15pm	P1142. Investigating overlay control towards 2.5/3D system integration in backend lithography processes *Huang, Chia-Ching (1); Lee, Yutai (1); Lee, Yuan-Chang (2); van der Krieken, Peter (1); Chang, Liang-Chuan (2); de Boeij, Jeroen (1); MISAT, Sylvain Irenee (1); Chang, Hsiang-Hung (2); van der Stam, Michiel (1)* Onto Innovation, Taiwan (1)	G2.4 (P1233) Novel Wet-Chemical Processing for Sidewall Plating of High Reliability Bottom-Terminated Packages *Hovestad, Arjan (1); Basu, Tarun (2)* Besi, The Netherland	G3.4 (P1240) Dielectric Breakdown of in-Package Epoxy Mold Compound under Wet and Dry Conditions: Frequency and Temperature dependence *Balestra, Luigi (1); Riaz, Muhammad Tanveer (1); Giuliano, Federico (1); Cavallini, Andrea (1); Reggiani, Susanna (1); Oldani, Luca (2); Guarnera, Simone Salvatore (2); Rossetti, Mattia (2); Depetro, Riccardo (2)* University of Bologna, Italy (1)	G4.4 (P12510 Semiconductor MEMS Waferbond Defect Detection: The Industrial Application of ResNets *Stoll, Fiete; Dubey, Vikas; Wünsch, Dirk; Roscher, Frank; Wiemer, Maik* ENAS Fraunhofer, Germany	G5.4 (P1109) Electrical Characterization and Reliability Studies of TSI with 5-layer Frontside Cu and 2-layer Backside Cu RDL *Tseng, Ya-Ching; Lau, Daniel; Ming, Calvin Chua Hung; Li, Hongyu* Institute of Microelectronics, Singapore	G6.4 (P1228) Fan-Out Packaging without Warpage *Schindler, Markus; Ringelstetter, Severin; Bues, Martin; Kreul, Kilian; Chian, Lim See; Königer, Tobias* Delo, Germany
2:15pm - 2:30pm	Tea Break & Exhibition (Grand Ballroom Foyer)					
Venue	Waterfront I	Waterfront II	Waterfront III	Riverfront I	Riverfront II	Riverfront III
2:30pm - 3:30pm	**H1. Assembly and Manufacturing Technology 3**	**H2. Quality, Reliability & Failure Analysis 3**	**H3. Materials and Processing 6**	**H4. Mechanical Simulation & Characterization 4**	**H5. Package Design and Characterization for AI Applications**	**H6. Flip Chip and Fan-Out on Substrate**
2:30pm - 2:50pm	H1.1 (P1346) Exploring Direct Laser Reflow Techniques for Forming Stable and Reliable Solder Bump Interfaces on Semiconductor Substrates *Fettke, Matthias; Fisch, Anne; Teutsch, Thorsten* PacTech, Germany	H2.1 (P1362) Lifetime modelling strategy for Multilayer Ceramic Capacitors by HALT test *Yang, Yongbo; Yong, Eric; Qiu, Wen* AMD, Singapore	H3.1 (P1279) Stress compensation effect in AlN/Mo/AlN/Polysilicon stack for MEMS application *Sharma, Jaibir; Qing Xin, Zhang* Institute of Microelectronics, Singapore	H4.1 (P1197) Dynamic Response of Interconnects in Board-level Packaging Structure at Extremely High Strain Rates *Long, Xu (1); Hu, Yuntao (2); Shi, Hongbin (3); Su, Yutai (2)* Northwestern Polytechnical University, China (1)	H5.1 (P1320) Process Development of Twin 2 Die Stack Modules for Deep Learning Hardware Accelerator *Ser Choong Chong* Institute of Microelectronics, Singapore	H6.1 (P1235) Fine-line RDL Structure Analysis of Fan-Out Chip-on-Substrate Platform *Lai, Chung-Hung* ASE Group, Taiwan
2:50pm - 3:10pm	H1.2 (P1366) Elimination of Compromised Wirebonding on Ceramic MEMS Package through Improved Process and Tooling Design *Bamba, Behra Esposo; Tabiera, Michael Tabiera; Gomez, Frederick Ray Gomez* STMicroelectronics, Philippines	H2.2 (P1257) Innovative Cu-Selective Passivation Coatings for Enhanced Reliability in Cu Interconnects for IC Packaging *Antony Jesu Durai, Kevin (1); Kumaravel, Dinesh Kumar (1); Muralidharan Nair, Shyam (1); Tran, Khanh (1); Chyan, Oliver (1); Poliah, Ramarao (2); Zhi Chan, Mei (3); Mathew, Varughese (4)* Univerity of North Texas, USA (1)	H3.2 (P1154) Die Attach Material Choice for MEMS Cavity Packages *Shaw, Mark; Simoncini, Daniele; Duca, Roseanne; Falorni, Luca; Carulli, Paola; Fedeli, Patrick; Brignoli, Davide* STMicroelectronics, Italy	H4.2 (P1242) Determination of the Adhesive Strength of Monocrystalline Layers as a Thin Film on a Silicon Substrate by Means of Instrumented Indentation Testing *Albrecht, Jan (1,2); Rzepka, Sven (1,2)* ENAS Fraunhofer, Germany (1)	H5.2 (P1398) Thermal Test Vehicles for Characterization of Thermal Performance of AI Chips *Shangguan, Dongkai (1); Yang, Cheng (2); Hang, Yin (3)* Thermal Engineering Associates (1)	H6.2 (P1131) The FOStrip® technique - a low-cost solution for the strip level fan-out on substrate package *Lin, I-Hung (1); Shih, Meng-Kai (2); Ding, Bo-Rui (2); Lou, Bai-Yao (1); Ni, Tom (1)* Kore Semiconductor Co., Ltd., Taiwan (1)
3:10pm - 3:30pm	H1.3 (P1351) Resolving Key Issues in Very Thin Die Package Manufacturing *Talledo, Jefferson; Tabiera, Michael; Graycochea Jr, Edwin* STMicroelectronics, Philippines	H2.3 (P1370) Embedded Defect Depth Estimation using NIR Model-less TSOM *Lee, Jun Ho (1); Joo, Ji Yong (1); Lee, Jun Sung (1); Kim, Se Jeong (1); Kwon, Oh-Hyung (2)* Kongju National University, South Korea	H3.3 (P1173) Enhancing Device Performance through Non-Pressure Sintering on Copper Lead frames *Danila, Bayaras, Abito; Balasubramanian, Senthil Kumar* Heraeus Materials Singapore	H4.3 (P1407) Electromigration Study of Cu Pillar Bumps Using Experimental and Numerical Methods *Zhao, Facheng; Zhu, Liping; Yeo, Alfred* STATS ChipPAC Singapore	H5.3 (P1261) Cost-Performance Co-Optimization for the Chiplet Era *Graening, Alexander Phillip (1); Patel, Darayus Adil (2); Sisto, Giuliano (2); Lenormand, Erwan (2); Perumkunnil, Manu (2); Pantano, Nicolas (2); Kumar, Vinay B.Y. (2); Gupta, Puneet (1); Mallik, Arindam (2)* UCLA, USA (1)	H6.3 (P1327) Semiconductor Chip and Package Co-Design and Assembly for Dual Use in FC and WB BGA *Rongrong Jiang; Trent Uehling, Bihua He; Tingdong Zhou; Meijiang Song; Azham Mohdsukemi; Taki Fang, Roy Lo; Kaelin Wang* NXP Semiconductor Company, China
3:30pm - 4:30pm	Interactive Poster Presentation III / Exhibitions / Coffee Break @ Waterfront foyer					
4:30pm - 5:00pm	**Closing Ceremony @ WaferFront Foyer**					
	Join our exciting lucky draw with many prizes to be won, including the grand prize of an iPhone 16 Plus!					